James Electronics Hardware Engineer

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EDUCATION MS – Electrical Engineering, 1990: Rutgers University, New Brunswick, NJ
BS – (Magna Cum Laude), Electrical Engineering, 1984: Rutgers University, New Brunswick, NJ

SUMMARY Results-oriented Electrical Engineering professional with over 20 years experience. Expertise in ***hardware design and program management.*** Exceptional technical and leadership skills.

- Defines architectures, establishes vendor relationships, ***designs boards and FPGAs***, and takes products through regulatory compliance into volume production.
- Leads aggressive cost reduction initiatives striking optimum balance between Cost reduction, Production risks and Time-To-Market needs.
- Significantly raised productivity levels by establishing procedures and design methodologies.
- Proven ability to build strong relationships with staff and supporting departments.
- Strong leader with motivational skills creating team cohesiveness and driving team results performance above individual abilities, consistently surpassing management expectations.
- Self-motivated and an innovative thinker, consistently pursuing new challenges to stretch abilities, expand knowledge, and bring greater returns to employers.

TECHNICAL QUALIFICATIONS:

- Technology: OC12, OC3, VDSL, ADSL, SDSL, DS3, T1, ISDN, SLIC, Compact PCI, Mini PCI, PCI Express, H.110, USB, Ethernet, ATM, IP, SAR, Utopia, POS PHY, LVDS, 802.11b/g Wireless, VoIP, LCD, ***FPGA***, ***CPLD***, RS-485, RS-422, RS-232, I2C, CP Gateway, Central Office (CO), Multiple Dwelling Units (MDU)
- Tools: Leonardo, ModelSim, ORCAD, Viewlogic, Agile, SAP, Actel, ***Xilinx***, ***Altera***, Quartus
- Software: Verilog HDL, C/C++
- Standards: NEBS, FCC, UL, DOC, IEC, CE, ANSI, EMI, EMC, ISO, RoHS

EXPERIENCE

ABC Corp. **Somewhere, NJ**

2/07 – present: Principal Engineer (contract position)

- Architects and designs VoIP cable modems and MDUs.
- Coordinates ODM suppliers and resolves engineering field issues.

DEF, Inc. **Somewhere, NJ**

2001 – 2/07: Senior Principal Engineer

- Led DSL hardware engineering developing Central Office, Customer Premise and R&D products. Designed first generation boards and FPGAs, prepared project plans and concurrently sustained management of 5 design efforts. Coordinated and motivated team of 7 engineers.
- Delivered to increasing needs with continuous staff reductions by establishing extended design groups in low cost design centers to handle overflow assignments and board builds. Instilled procedures enabling autonomous site operation with common design tools, milestones and deliverables. Set competency expectations by writing design guidelines for high-speed digital, sensitive analog front-ends and regulatory compliance.
- Accelerated product revenue by 6 months for new DSL Central Office chipsets and streamlined continued engagements by designing high density Tier 1 Line Cards and documenting statement of work procedures.
- Designed DSL VoIP wireless gateways and obtained FCC certification. Developed and maintained vendor relationships for support peripherals and power supplies based on cost, performance and availability. Reduced design risk and accelerated subsequent board designs by creating reusable functional schematic and layout templates.
- Solved Customer Premise gateway design and manufacturing issues for Taiwanese and Chinese ODMs accelerating product launch and revenues.
- Eliminated expensive test equipment infrastructure needs by leading development of network and embedded processor R&D systems. Designed Altera FPGAs and CPLDs with Verilog HDL and ModelSim simulation to implement processor glue logic, timing domain synchronization, real-time data capturing, UARTs and LCD controllers.
- Improved software integration and LSI validation robustness by defining IP network processor architectures and leading product development of ADSL and VDSL Multiple Dwelling Units.
- Accelerated design and procurement cycles by spearheading Company standardization of RoHS component databases and procedures for ORCAD, PCAD, Agile and SAP.

GHI Company, Inc. **Somewhere, NJ**

1999 – 2001: Principal Staff Engineer

- Managed team of 3 engineers through two generations of Central Office access equipment. Set technical direction by specifying hardware data flows, board partitioning and establishing key OEM relationships. Designed line cards, embedded processors and data path FPGAs.
- Met milestones by containing design effort within available resources by selecting and fostering Motorola OEM relationship gaining early access to their high availability Compact PCI chassis and controller technologies.
- Designed OC-12 ATM Uplink, Quad ATM DS3 Line Card and Host Processor board. Researched and selected PMC-Sierra optical and wired data communication PHYs, Motorola 8240 PowerPC, Mindspeed SAR, MMC switch fabric, LVDS backplane links and Intel CPCI bridges.
- Interfaced incompatible data paths and processor busses by writing Verilog HDL for Xilinx FPGAs and CPLDs.

LoL **Somewhere, NJ**

1995 – 1999: Senior Member of Technical Staff

- Defined H.110 SCSA embedded backplane architecture and designed NEBS compliant hardware and C software for Central Office products. Provided design support sustaining volume production and revenue stream for legacy channel bank equipment.
- Designed the system's first board, Quad ISDN BRI. Defined the Philips embedded processor core and wrote software drivers used on all subsequent board designs.
- Consolidated multi-chip ISDN to 3DS0 conversion logic by designing a single Xilinx FPGA reducing legacy two board solutions to a single line card.
- Researched DSL vendors based on density, power, features and technical support. Designed SDSL Line Card and integrated third party firmware for Central Office and Remote Terminal applications.
- Translated transceiver's slotted data output to RS-422 clear channel format by writing Verilog HDL to buffer and retime data streams.
- Resolved EMC and EMI compliance issues on line cards and backplane obtaining NEBS certification.

MO, Inc. **Somewhere, NJ**

1990 – 1995: Lead Staff Engineer

- Designed Intel and Motorola embedded controllers and V.32bis and V.22bis voice modems with Actel FPGAs for T1 multiplexer and protection relay equipment.

BRB Corp. **Somewhere, NJ**

1984 – 1990: Lead Design Engineer

- Designed, debugged and integrated embedded processor, DSP and timing boards for imaging guidance systems.

PROFESSIONAL AFFILIATIONS

IEEE, Active Member
The Tau Beta Pi Association, Member
Eta Kappa Nu Honor Society